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AF/2813

Docket No.: 50432-104 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In Application of	:	Customer Number: 20277
Suzette K. PANGRLE, et al.	:	Confirmation Number: 2391
Serial No.: 10/073,066	:	Group Art Unit: 2813
Filed: February 12, 2002	:	Examiner: Thanh Nguyen

For: PHOSPHINE TREATMENT OF LOW DIELECTRIC CONSTANT MATERIALS IN SEMICONDUCTOR DEVICE MANUFACTURING

TRANSMITTAL OF APPEAL BRIEF

Mail Stop Appeal Brief
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith in triplicate is Appellant(s) Appeal Brief in support of the Notice of Appeal filed October 1, 2003. Please charge the Appeal Brief fee of $330.00 to Deposit Account 500417.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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Sir:

This Appeal Brief is submitted in support of the Notice of Appeal filed October 1, 2003.

I. REAL PARTY IN INTEREST

The real party in interest is Advanced Micro Devices, Inc.

II. RELATED APPEALS AND INTERFERENCES

Appellants are unaware of any related appeals and interferences.

III. STATUS OF CLAIMS

Claims 1-8 and 10-17 are pending in the application, of which claims 16 and 17 have been withdrawn from consideration pursuant to 35 U.S.C. § 121 and claim 21 has been cancelled without prejudice thereto. Claims 1-8 and 10-15 have been finally rejected. It is from the final rejection of claims 1-8 and 10-15 that this Appeal is taken.

IV. STATUS OF AMENDMENTS

No other Amendment has been filed subsequent to the final Office Action dated July 8, 2003. No request for reconsideration was made subsequent to the final Office Action.

V. SUMMARY OF INVENTION

The present invention stems from the discovery that the surface properties of a material having a low dielectric constant (low k), which is useful in semiconductor fabrication, can be improved by exposing the surface of the low k dielectric layer to phosphine and/or a plasma containing a phosphine source. The present invention thus provides methods for modifying the surface of a low k dielectric and has utility in the fabrication of integrated semiconductor devices. (See, e.g., page 5, lines 1-7 of the present specification)

It has been noted that many of the difficulties in the employment of low k materials lie in the surface properties of the low k dielectric layer. For example, it has been observed that, under certain circumstances, adding a protective capping layer on a low k dielectric layer results in poor adhesion. It

has been observed that applying the capping layer by conventional plasma deposition techniques can cause an underlying low k layer, particularly a porous dielectric underlayer, to degrade due to the oxidation attendant during the formation of the capping layer. The degradation is due to bond breaking and loss of hydrogen and/or methyl groups in such materials when oxygen or oxygen radicals react with the surface of an underlying low k layer. (See, e.g., page 3, lines 1-8 of the present specification)

In accordance with the present invention, the improvement in the surface properties is carried out by subjecting a surface of the low k dielectric to phosphine and/or a phosphine plasma and subsequently forming a cap layer directly on the treated surface of the dielectric layer.

VI. ISSUES

A. The Rejection

Claims 1-4, 6-8 and 10-15 were rejected under 35 U.S.C. § 103(a) for obviousness predicated upon Usami (U.S. Patent No. 6,133,137) in view of Mikagi (U.S. 6,153,507). Claim 5 was rejected under 35 U.S.C. § 103(a) for obviousness predicated upon Usami in view of Mikagi and further in view of Shin (U.S. Patent No. 6,376,876).

B. The Issue That Arises In This Appeal And Requires Resolution By The Honorable Board of Patent Appeals And Interferences (The Board) Is:

Whether claims 1-4, 6-8 and 10-15 are unpatentable under 35 U.S.C. § 103(a) for obviousness predicated upon Usami in view of Mikagi; and whether claim 5 is unpatentable under 35 U.S.C. § 103(a) for obviousness predicated upon Usami in view of Mikagi and further in view of Shin.

VII. GROUPING OF CLAIMS

The appealed claims do not stand or fall together as a group. The patentability of claims 1-4, 6-8 and 10-15 stand or fall together as a group; the separate patentability of claim 5 is advocated.

VIII. THE ARGUMENT

It is Appellants' position that the imposed rejection under 35 U.S.C. § 103 is factually and legally erroneous for several reasons.

A. Factual Error In Interpretation Of Primary Reference

Independent claim 1 is directed to a method of forming a composite dielectric on a semiconductor substrate. The method comprises forming a low k dielectric layer having an exposed surface on the substrate; treating the exposed surface of the dielectric layer with phosphine and/or a phosphine plasma; and forming a cap layer directly on the treated surface of the dielectric layer. The claim requires that the cap layer is a dielectric and formed in-situ after treating the exposed surface of the dielectric layer. Dependent claim 5 further specifies the cap layer.

The primary reference, Usami, does not teach forming a cap layer directly on a treated surface of a low k dielectric layer. In fact, Usami shows the opposite. Usami treats side surfaces of a via hole and then contacts the treated surface with a conductive material rather than a cap dielectric layer.

In the final Office Action on page 3, fifth full paragraph, the Examiner asserts that layer 107 (layer 107 is shown in figure 2 of Usami) qualifies as a dielectric layer. It is not. Layer 107 in Usami is a conductor. Accordingly, it is respectfully submitted that the Examiner's interpretation of Usami is in error.

As shown in Figure 2 of Usami, the structure consists of second metal wiring pattern 108 over via plug 107 which is in electrical communication with first metal wiring pattern 102. (See, e.g., column 4, lines 1-5 of Usami) Wire patterns 108 and 102 are isolated from each other by insulating films 105, 104 and 103. Insulating film 104 was subjected to a hydrogen plasma creating treated surfaces 106. It is noted that Usami teaches that phosphine can be substituted for the hydrogen plasma on column 5, lines 34-41. Nevertheless, via plug 107 is a conductor which functions to electrically connect wire patterns 108 to 102. Usami teaches on column 4, line 17, that via plug 107 can be formed from tungsten, aluminum, and copper – all conductors. Nowhere in Usami is there the disclosure of forming a cap dielectric layer directly on a phosphine treated surface.

This gap between the claimed subject matter and the process taught by Usami is not bridged by the secondary references. Hence, even if the applied references are combined, the claimed methods would not result. *Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 5 USPQ2d 1434 (Fed. Cir. 1988).* Thus, the Examiner's rejection under 35 U.S.C. § 103 is predicated upon clear factual error.

B. The Examiner Has Not Established The Requisite Motivation To Negative Patentability Of Claims 1-4, 6-8, 10-15

Appellants rely upon a basic procedural tenet repeatedly applied by the Court of Appeals for the Federal Circuit. Specifically, in order to establish the requisite motivation, the Examiner must make "clear and particular" factual findings as to a specified understanding or specific technological principle which would have realistically impelled one having ordinary skill in the art to modify a particular reference (Usami's method) to arrive at the claimed invention based upon facts. *Ruiz v. A.B. Chance Co., 234 F.3d 654, 57 USPQ2d 1161 (Fed. Cir. 2000); Ecolochme Inc. v. Southern California Edison, Co., 227 F.3d 1361, 56 USPQ2d 1065 (Fed. Cir. 2000); In re Kotzab, 217 F.3d 1365, 55 USPQ 1313 (Fed. Cir. 2000); In re Dembiczak, 175 F.3d 994, 50 USPQ2d 1614 (Fed. Cir. 1999).* Moreover, and

quite significantly, the Examiner is required to explain why one having ordinary skill in the art would have been realistically motivated to modify Usami's particular method and device to arrive at the claimed invention. *Ecolochem Inc. v. Southern California Edison, Co., supra; In re Rouffet, 149 F.3d 1350, 47 USPQ2d 1453 (Fed. Cir. 1998).* The Examiner has failed to meet this burden.

Rather, the Examiner has merely identified some features in the secondary reference to Mikagi such as show in figure 6A-6C. Therein, Mikagi shows forming a silicon dioxide layer 104b, treating the silicon dioxide layer with a phosphine plasma 109a, annealing the treated layer 104b to form an impurity containing silicon dioxide layer 108a, and forming another silicon dioxide layer 110a over 108a. See also column 8, beginning at line 15. At column 8, lines 29-32, Mikagi teaches that a low dielectric film can be substituted for the silicon dioxide film 104b. However, Mikagi does not describe forming a cap layer, in-situ, after treating the exposed surface of a low k dielectric layer.

In the final Office Action on page 4, second to last line, the Examiner asserted that Mikagi taught the feature of an in-situ process. Appellants respectfully disagree. Mikagi is silent on this point. Silence in a reference is not a disclosure of facts. *In re Burt*, 356 F.2d 115, 148 USPQ 548 (CCPA 1966).

Mikagi may suggest using similar processes in forming various dielectric layers. However, the fact that similar processes are described does not equate to in-situ process, let alone claim 1. This is particularly true with Mikagi. This reference in fact teaches the step of annealing a treated silicon dioxide layer (Col. 8, beginning at line 45). There is no indication that this step can occur such that a cap layer can be formed in-situ, let alone the method of claim 1 as a whole. Merely identifying features of a claimed invention perceived to reside in disparate references does not render the claimed invention as a whole obvious within the meaning of 35 U.S.C. § 103. *In re Kotzab, supra.; Grain Processing Corp. v. American-Maize Products Co., 840 F.2d 902, 5 USPQ2d 1788 (Fed. Cir. 1988).* The

Examiner has not explained why one having ordinary skill in the art would have been realistically motivated to modify Usami's particular method and semiconductor device to arrive at the claimed invention based upon "clear and particular" factual findings in the applied prior art, regardless of what the Examiner may perceive as the source of motivation. *Ecolochem Inc. v. Southern California Edison, Co., supra.; In re Rouffet, supra.*

C. Claim 5 is Patentable within the Meaning of 35 U.S.C. § 103(a)

Nether Usami nor Mikagi teach or suggest forming a cap layer selected from the group consisting of silicon nitride, silicon oxynitride, silicon carbide and composites thereof, let alone forming such a cap layer in the process of independent claim 1. To bridge this gap, the Examiner asserted (page 6, second full paragraph of the final Office Action) that forming a cap layer from this group are known in semiconductor processing as evidenced by Shin. Therefore, according to the Examiner, it would have been obvious to the skilled artisan at the time of the invention to use such materials because using such materials would protect the underlayer. These assertions are factually and legally erroneous.

First, there is no evidence that using a cap layer would necessarily protect the underlayer. There is no basis in the record to make this statement. Even if this were correct, the underlayer taught in Shin is the opposite of the primary references. Shin shows, in Figure 5B, cap layer 32s over, dummy gate electrode 30s. The gate electrode is over inter dielectric layer 28s, which in turn is over gate electrode 26s. See also column 8, beginning at line 17. The cap layer of Shin is over a conducting material, i.e., electrode 30s. Usami teaches isolating conductors and Mikagi teaches forming a series of insulators. There is no basis in the record to support the conclusion that the underlayer of Shin, a conductor, would have the same problems and employ the same solutions as the underlayers of Usami

or Mikagi, which are insulators, let alone the problems addressed by the claimed methods.

Second, there is no reason why one or ordinary skill in the art, having the cited references in hand, would be motivated to modify the specific teachings of Usami or Mikagi with that of Shin. To the contrary, Usami and Mikagi relate to interwiring structures and methods therefore, while Shin relates to flash memory devices. The structure of Shin is not related to a interconnected wiring pattern structure, as shown in Usami. There is no basis in the record to support the conclusion that one skilled in the art would have replaced the cap layer over the electrode shown in Shin with the insulating layers shown in Usami or Mikagi.

In order to establish the requisite realistic motivation, the Examiner must make a "thorough and searching" factual inquiry and, based upon that factual inquiry, explain why one having ordinary skill in the art would not have been realistically impelled one modify particular prior art, in this case, the acknowledged prior art methodology, to arrive at the claimed invention. *In re Lee, 237 F.3d 1338, 61 USPQ2d 1430, 1433 (Fed. Cir. 2002).* That burden has not been discharged.

IX. CONCLUSION

Appellants, therefore, respectfully submit that the Examiner has not established a *prima facie* basis to deny patentability of the claimed methods as a whole under 35 U.S.C. § 103.

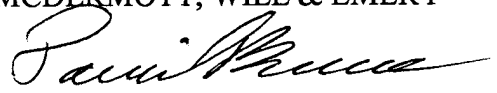
X. PRAYER FOR RELIEF

Based upon the arguments presented, it is apparent that one having ordinary skill in the art would not have found the claimed invention as a whole obvious within the meaning of 35 U.S.C. § 103. Appellants, therefore, respectfully solicit the honorable Board to reverse the Examiner's imposed rejection under 35 U.S.C. § 103.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY



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XI. APPENDIX

1. A method of forming a composite dielectric on a semiconductor substrate, the method comprising:

forming a low k dielectric layer having an exposed surface on the substrate;

treating the exposed surface of the dielectric layer with phosphine and/or a phosphine plasma; and

forming a cap layer directly on the treated surface of the dielectric layer, wherein the cap layer is a dielectric and formed in-situ after treating the exposed surface of the dielectric layer.

2. The method of claim 1, comprising forming the dielectric by spin-on-glass techniques.

3. The method of claim 1, comprising introducing the substrate to a plasma enhanced chemical vapor deposition (PECVD) chamber having a phosphine source to treat the exposed surface of the dielectric layer.

4. The method of claim 3, comprising introducing phosphine together with a carrier gas to the PECVD chamber as the phosphine source.

5. The method of claim 3, wherein the cap layer is selected from the group consisting of silicon nitride, silicon oxynitride, silicon carbide and composites thereof.

6. The method of claim 1, comprising patterning a photoresist on the cap layer and etching through the cap and dielectric layers to expose side surfaces of the cap and dielectric layers.

7. The method of claim 6, comprising subjecting the exposed side surfaces of the cap and dielectric layers to a phosphine plasma.

8. The method of claim 1, comprising forming the dielectric layer from a silsesquioxane dielectric material or derivative thereof.

10. The method of claim 6, comprising

removing the photoresist layer; and

forming a conformal barrier layer on the dielectric layer including the phosphine plasma treated side surfaces thereof.

11. The method of claim 10, comprising forming a conductive layer comprising copper on the conformal barrier layer and within the etched dielectric layer.

12. The method of claim 11, comprising polishing the conductive layer to the barrier layer to form a conductive trench or plug within the dielectric layer.

13. The method according to claim 12, comprising forming a cap layer over the conductive layer and barrier layer.

14. The method according to claim 1, wherein the dielectric layer comprises a porous silicon oxide.

15. The method of claim 14, comprising depositing the silicon oxide at a thickness of about 0.3 microns to about 1 micron.